DTμL9935
HEX INVERTER
DIODE-TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION

The 9935 is an expandable CCSL Hex Inverter. It consists of six DTμL gates without input diodes which are expandable by using external diodes or by using the DTμL 9933 Dual 4-Input Extender element. It is ideal for a wide variety of applications, including one-shot multivibrators, latching circuits, flip-flops, adders, registers, counters, decoders and many more.

FEATURES

- Expandable Inputs
- Wired-OR Capability
- The input/output characteristics provide easy interfacing with Fairchild LPDTμL, TTμL and MSI families (CCSL).
- All ceramic "HERMETIC" 14-pin Dual In-Line and CERPAK packages

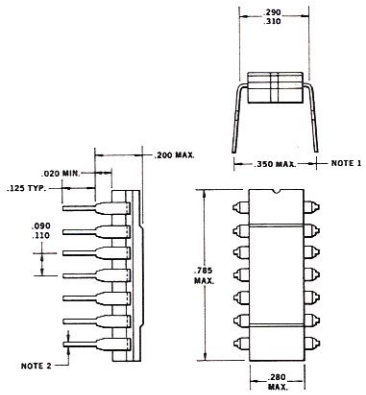
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambrient) Under Bias	-55°C to +125°C
V_{CC} Pin Potential to Ground Pin	-0.5 V to +8 V
Input Voltage	-1.5 V to Input Diode Breakdown
Voltage Applied to Outputs (Inputs Low)	-0.5 V to V_{CC} Value
Current Into Output When Output is Low	30 mA

ORDER INFORMATION

Specify U3I99355XX for flat package and U6A99355XX for Dual-In-Line package, where 5XX is 51X for -55°C to +125°C temperature range or 59X for the 0°C to +75°C temperature range.

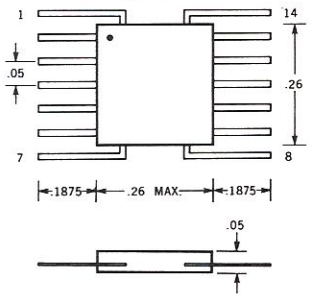
TYPICAL DUAL IN-LINE PACKAGE



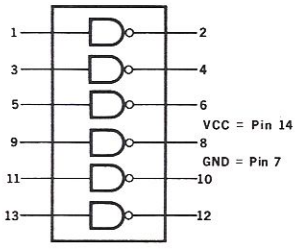
NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

TYPICAL FLAT PACKAGE

TOP VIEW



LOGIC DIAGRAM



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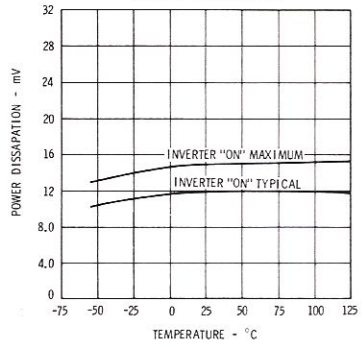
ELECTRICAL CHARACTERISTICS

SYMBOL	CHARACTERISTIC	-55°C MIN	-55°C TYP	-55°C MAX	+25°C MIN	+25°C TYP	+25°C MAX	+125°C MIN	+125°C TYP	+125°C MAX	UNITS	CONDITIONS & COMMENTS V_{CC} = 5.0 V ± 10%
V_{OH}	Output High Voltage	2.6			2.6	3.3		2.5			Volts	V_{CC} = 4.5V, I_{OH} = -180μA
V_{OL}	Output Low Voltage			0.4		0.3	0.4			0.4	Volts	V_{IL} = Value indicated on this Table V_{CC} = 5.5V, I_{OL} = 15 mA V_{CC} = 4.5V, I_{OL} = 12 mA
V_{IH}	Input High Voltage	2.3			2.0			1.8			Volts	Input High Threshold with FD600 on Input
V_{IL}	Input Low Voltage			1.4			1.1			0.8	Volts	Input Low Threshold with FD600 on Input
I_F	Input Load Current			-1.5			-1.5			-1.5	mA	V_{CC} = 5.5V, V_F = 0.4
I_F	Input Load Current			-1.2			-1.2			-1.2	mA	V_{CC} = 4.5V, V_F = 0.4
t_{pd+}	Turn-Off Delay				25	65	80				ns	SEE Figure. 4
t_{pd-}	Turn-On Delay				10	30	40				ns	SEE Figure 4

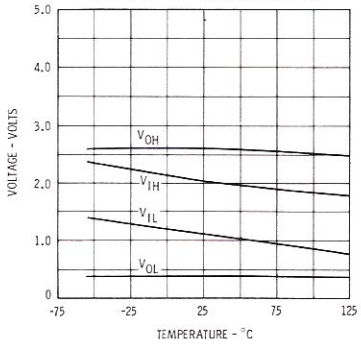
SYMBOL	CHARACTERISTIC	0°C MIN	0°C TYP	0°C MAX	25°C MIN	25°C TYP	25°C MAX	75°C MIN	75°C TYP	75°C MAX	UNITS	CONDITIONS & COMMENTS V_{CC} = 5.0 V ± 5%
V_{OH}	Output High Voltage	2.6			2.6			2.5			Volts	V_{CC} = 4.75, I_{OH} = -180μA
V_{OL}	Output Low Voltage			0.45			0.45			0.45	Volts	V_{IL} = Value indicated on this Table V_{CC} = 5.25V, I_{OL} = 15.2 mA V_{CC} = 4.75V, I_{OL} = 13.3 mA
V_{IH}	Input High Voltage	2.1			2.0			1.85			Volts	Input High Threshold with FD600 on Input
V_{IL}	Input Low Voltage			1.2			1.1			0.95	Volts	Input Low Threshold with FD600 on Input
I_F	Input Load Current			-1.52			-1.52			-1.52	mA	V_{CC} = 5.25V, V_F = 0.45
I_F	Input Load Current			-1.33			-1.33			-1.33	mA	V_{CC} = 4.75V, V_F = 0.45
t_{pd+}	Turn-Off Delay				25	65	80				ns	SEE FIGURE 4
t_{pd-}	Turn-On Delay				10	30	40				ns	SEE FIGURE 4

CURVES FOR −55°C TO +125°C TEMPERATURE RANGE

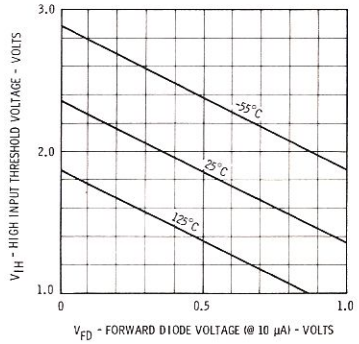
WORST CASE POWER DISSIPATION VERSUS TEMPERATURE (EACH INVERTER)



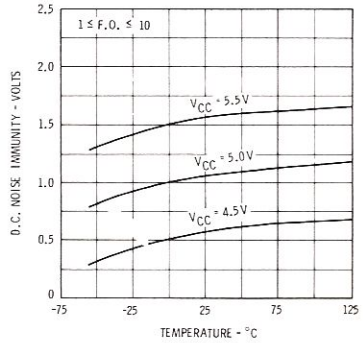
WORST CASE OPERATING VOLTAGE CHARACTERISTICS



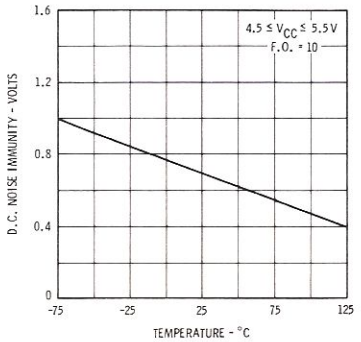
V_{IH} THRESHOLD VERSUS FORWARD DIODE VOLTAGE



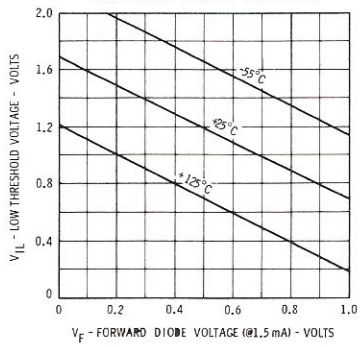
WORST CASE HIGH LEVEL NOISE IMMUNITY VERSUS TEMPERATURE



WORST CASE LOW LEVEL NOISE IMMUNITY VERSUS TEMPERATURE

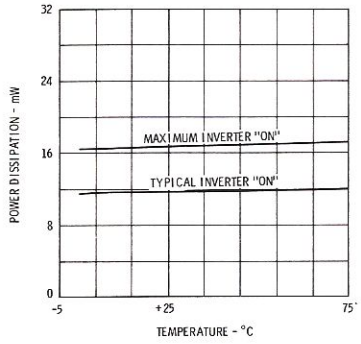


V_{IL} THRESHOLD VERSUS FORWARD DIODE VOLTAGE

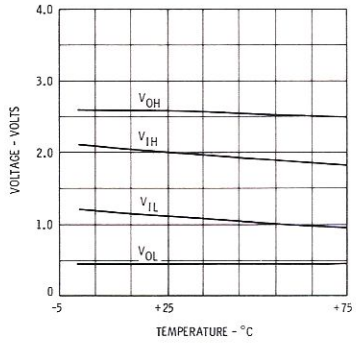


CURVES FOR 0°C TO +75°C TEMPERATURE RANGE

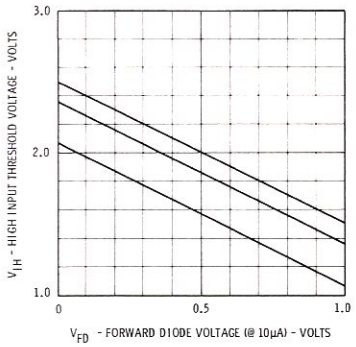
WORST CASE POWER DISSIPATION VERSUS TEMPERATURE (PER INVERTER)



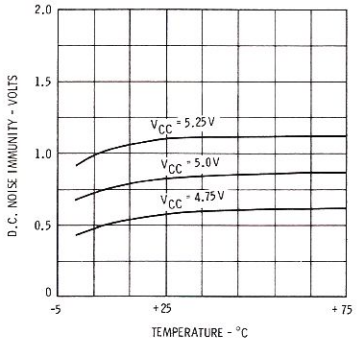
WORST CASE OPERATING VOLTAGE CHARACTERISTICS



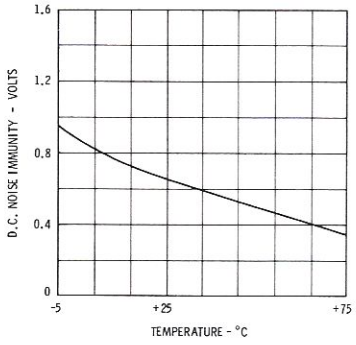
V_{IH} THRESHOLD VERSUS FORWARD DIODE VOLTAGE



WORST CASE HIGH LEVEL NOISE IMMUNITY



WORST CASE LOW LEVEL NOISE IMMUNITY VERSUS TEMPERATURE



V_{IL} THRESHOLD VERSUS FORWARD DIODE VOLTAGE

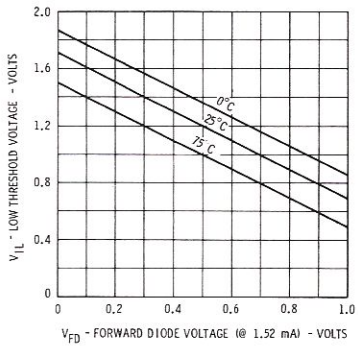


FIG. 1

SCHEMATIC DIAGRAM (ONE INVERTER ONLY)

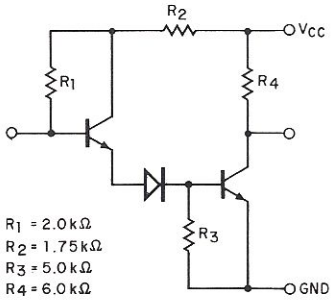


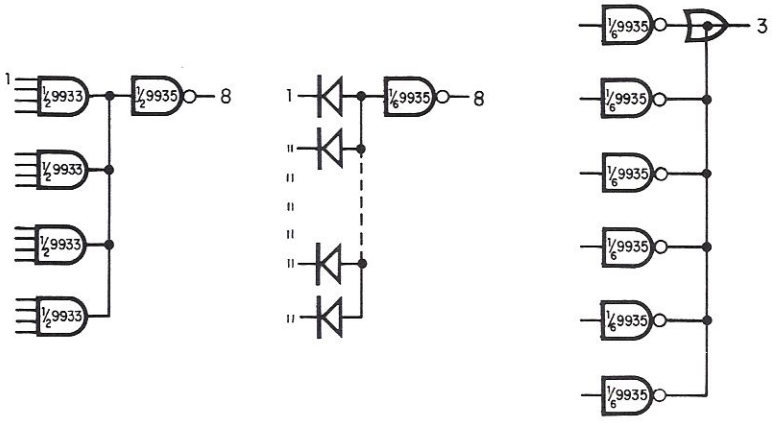
FIG. 2

LOADING RULES

OUTPUT STATE	FANOUT 51X	59X
HIGH	10	10
LOW	10	10

FIG. 3

RULES FOR INPUT EXPANSION AND "WIRED OR" CONNECTION



6 x 1/6 9935 "WIRED OR" For the "WIRED OR" function - Subtract 1 unit fan-out for each added gate. Subtract 5 fan-outs for 6 added gates.

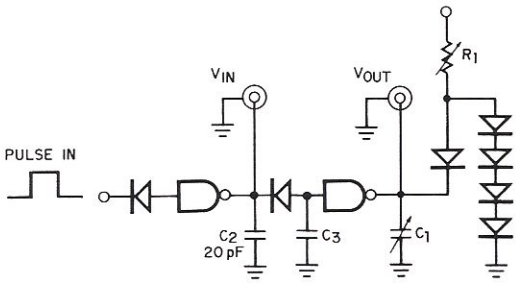
EXPANSION OF INPUTS

Typical input capacitance of the 9933 is 2.0 pF and output capacitance is 5.0 pF. All wiring should be kept as possible to minimize effects of distributed capacitance on circuit performance.

Use FD600 or equivalent expansion.

FIG. 4

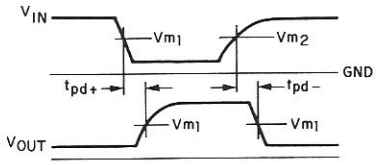
SWITCHING TIME TEST CIRCUIT



Diodes are FD600

	t_{pd+}	t_{pd-}
R_1	3.9k	400Ω
C_1	30pF	50pF
C_2	20pF	20pF
C_3	5 pF	5 pF

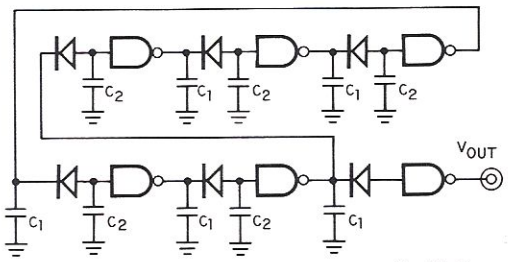
(INCLUDES JIG & PROBE CAPACITANCE)



TEMP.	V_{m1} (VOLTS)	V_{m2} (VOLTS)
−55°C	1.7	1.5
+25°C	1.5	1.3
+125°C	1.3	1.1

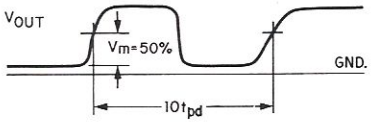
FIG. 5

RING CIRCUIT FOR MEASURING AVERAGE PROPOGATION DELAY

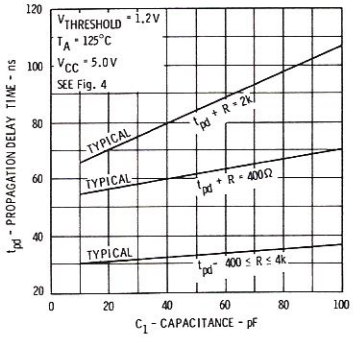


C_1 = 30 pF
C_2 = 5pF
(INCLUDES JIG & PROBE CAPACITANCE)

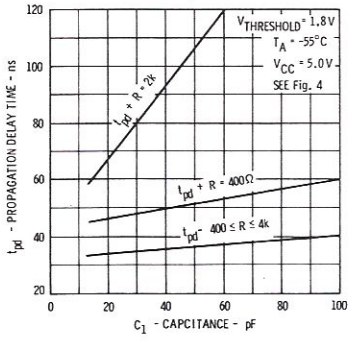
Diodes are FD600



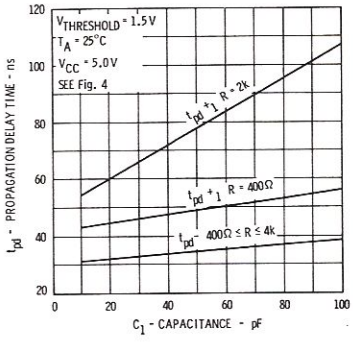
PROPAGATION DELAY VERSUS CAPACITANCE AT +125°C



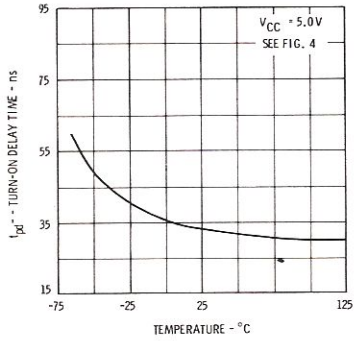
PROPAGATION DELAY VERSUS CAPACITANCE AT +25°C



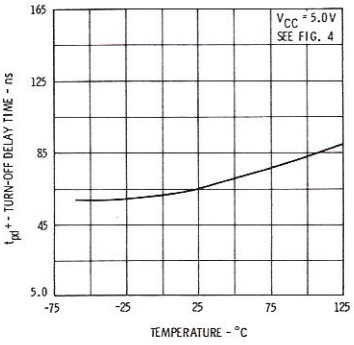
PROPAGATION DELAY VERSUS CAPACITANCE AT −55°C



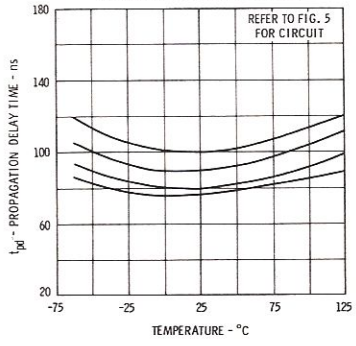
TYPICAL TURN-ON DELAY (t_{pd-}) VERSUS TEMPERATURE



TYPICAL TURN-OFF DELAY (t_{pd+}) VERSUS TEMPERATURE



MAXIMUM PROPAGATION DELAY VERSUS TEMPERATURE



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